

## CLAIMS

What is claimed is:

- 1 1. A method comprising:
  - 2 electrically connecting a first kicker device to a first drain bias for a first
  - 3 non-volatile memory cell, wherein said first kicker device comprises a
  - 4 high performance transistor;
  - 5 enabling said first kicker device; and
  - 6 pulling a voltage of said first drain bias towards a voltage potential of a supply
  - 7 source.
- 1 2. The method of claim 1, wherein said first non-volatile memory cell is a flash
- 2 memory cell.
- 1 3. The method of claim 1, wherein said high performance transistor is a p-channel
- 2 semiconductor device.
- 1 4. The method of claim 1, wherein said first kicker device is enabled prior to sensing
- 2 the contents of said first non-volatile memory cell.
- 1 5. The method of claim 1, wherein:
  - 2 said first non-volatile memory cell is included in a data array;
  - 3 a second kicker device is electrically connected to a second drain bias for a
  - 4 second non-volatile memory cell;
  - 5 said second non-volatile memory cell is included in a reference array; and

6       said first kicker device and said second kicker device pull a voltage of a sense  
7                  node for said first non-volatile memory cell and a voltage of a reference  
8                  node for said second non-volatile memory cell towards the same voltage  
9                  potential.

1     6.   The method of claim 1, wherein said first drain bias comprises a cascode  
2                  amplifier.

1     7.   A kicker for a non-volatile memory drain bias circuit, comprising:  
2                  a high performance transistor, wherein a first terminal of said high performance  
3                  transistor receives a voltage from a supply voltage and a second terminal  
4                  of said high performance transistor provides a voltage to said non-volatile  
5                  memory drain bias circuit; and  
6                  an enable signal, wherein said enable signal activates said high performance  
7                  transistor.

1     8.   The kicker for a non-volatile memory drain bias circuit of claim 7, wherein said  
2                  non-volatile memory drain bias circuit provides the drain bias for a flash memory  
3                  cell.

1     9.   The kicker for a non-volatile memory drain bias circuit of claim 7, wherein said  
2                  high performance transistor is a p-channel semiconductor device.

1     10.   The kicker for a non-volatile memory drain bias circuit of claim 7, wherein said  
2                  kicker pulls the voltage of a node towards the voltage potential of a supply source.

1 11. The kicker for a non-volatile memory drain bias circuit of claim 7, wherein said  
2 kicker is enabled prior to sensing the contents of a first non-volatile memory cell.

1 12. The kicker for a non-volatile memory drain bias circuit of claim 11, wherein:  
2 said first non-volatile memory cell is included in a data array;  
3 a second kicker is electrically connected to a second drain bias for a second  
4 non-volatile memory cell;  
5 said second non-volatile memory cell is included in a reference array; and  
6 said kickers pull a sense node for said first non-volatile memory cell and a  
7 reference node for said second non-volatile memory cell towards the same  
8 voltage potential.

1 13. The kicker for a non-volatile memory drain bias circuit of claim 7, wherein said  
2 non-volatile memory drain bias circuit comprises a cascode amplifier.

1 14. A non-volatile memory device, comprising:  
2 a first drain bias circuit for a first memory cell;  
3 a first kicker circuit for said first drain bias circuit, wherein said first kicker circuit  
4 comprises a high performance transistor and wherein said first kicker  
5 circuit pulls the voltage of a node towards a voltage potential of a supply  
6 source.

1 15. The non-volatile memory device of claim 14, wherein said non-volatile memory  
2 device is a flash memory device.

- 1 16. The non-volatile memory device of claim 14, wherein said high performance  
2 transistor is a p-channel device.
- 1 17. The non-volatile memory device of claim 14, wherein said first kicker circuit acts  
2 as a low resistance path to said supply voltage and said first kicker circuit charges  
3 the bitline for said first memory cell.
- 1 18. The non-volatile memory device of claim 14, wherein said first kicker circuit is  
2 enabled prior to sensing the contents of said first memory cell.
- 1 19. The non-volatile memory device of claim 14, further comprising:  
2 a second drain bias circuit for a second memory cell; and  
3 a second kicker circuit for said second drain bias circuit, wherein:  
4 said first memory cell is included in a data array;  
5 said second memory cell is included in a reference array; and  
6 said first kicker circuit and said second kicker circuit pull a sense node for  
7 said first memory cell and a reference node for said second  
8 memory cell towards the same voltage potential.
- 1 20. The non-volatile memory device of claim 14, wherein said first drain bias circuit  
2 comprises a cascode amplifier.